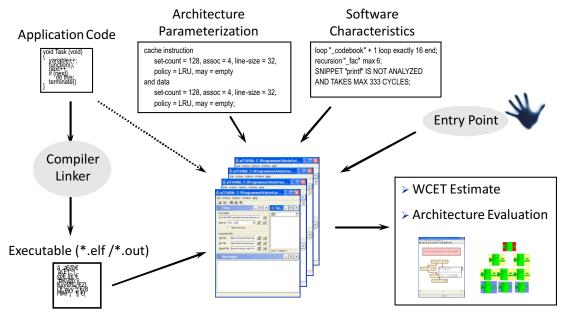
TimingExplorer

Exploring Timing Effects at Early Design Stages

TimingExplorer offers a set of **parameterizable ECU core models** to explore the effects of different ECUs or different ECU configurations on the worst-case execution time performance. This allows designers to **account for timing** and timing effects in an **early design phase** and helps to avoid late-stage integration problems.



The Challenge:

Choosing a **suitable processor configuration** at the beginning of the development is a challenge. A configuration which is too powerful can lead to a waste of expensive resources. A configuration not powerful enough might entail changes late in the development cycle and delay the delivery.

The Technique:

- TimingExplorer offers a set of basic ECU core models representative for different performance classes. Cache architecture and memory map are fully parameterizable.
- TimingExplorer requires representative source code of representative application parts, e.g. from previous releases or rapid-prototyping development environments.
- The source code is compiled by a standard compiler and its timing behavior is determined using AbsInt's aiT timing analysis technology.

Your Benefit:

- TimingExplorer is a building block for ECU-level architecture exploration. It helps designers to make informed decisions with respect to which ECU architectures are appropriate for an application at an early stage of product development.
- TimingExplorer is focused on the worst-case timing and automatically provides 100% coverage on the analyzed software so that critical corner cases are automatically considered.
- The effects of different ECU types and configurations can be evaluated without the need to have the physical hardware available. This helps to prevent late-stage integration problems.



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