a³ - AbsInt Advanced Analyzer

a³ provides a **common graphical user interface** to **all AbsInt analyzers** working on **binary code**. It enables users to **interactively explore** analysis results, to save and restore analysis scenarios, and offers fully integrated graphical and textual viewers for control flow, analysis results, source code, assembly code, and configuration files. All tools can be handled with the same look and feel and benefit from the same **powerful visualization features**, thus enabling an **efficient analysis process**.

aiT WCET Analyzer

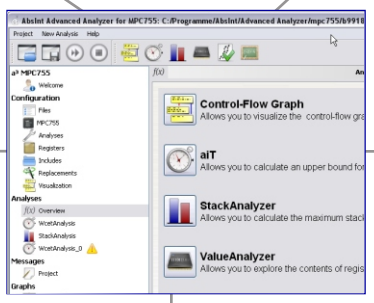
computes safe upper bounds on the worst-case execution time of tasks in real-time systems. The computed bounds are valid for all inputs and each task execution. aiT-computed bounds are tight and reflect the real performance of your system. Cache and pipeline effects are fully taken into account. Ensuring deadline adherence is no longer done at the expense of hardware resources.

ValueAnalyzer

automatically determines which memory areas are read or written by the tasks of your application. This allows to validate that the tasks only access storage they are allowed to access and that task-local storage cannot be corrupted by other tasks. The values of registers and memory cells are shown at each program point supporting validation/certification activities at the program assembly or binary level.

TimeWeaver

computes task-level WCET estimates from the execution time of code snippets obtained from real-time instruction-level tracing. The computed time bounds provide valuable feedback for optimizing worst-case performance.



StackAnalyzer

computes safe and precise upper bounds of the maximum stack usage of tasks. Stack height differences are shown as annotations in the call graph and control flow graph. The analysis results are valid for all inputs and for each task execution.

TimingExplorer

offers a set of parameterizable ECU core models to explore the effects of different ECUs or different ECU configurations on the worst-case execution time performance. This allows designers to account for timing effects in an early design phase and helps to avoid late-stage integration problems.

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